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2123

PATENT 9200

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of

Yu-Chin HSU et al

Art Unit: 2123

Application No: 09/630,348

Examiner:
Kandasamy Thangavelu

Filed: July 31, 2000

For: CIRCUIT PROPERTY VERIFICATION SYSTEM

PETITION TO WITHDRAW HOLDING OF ABANDONMENT

COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450

Sir:

The Notice of Abandonment mailed December 23, 2004 indicates that applicant failed to file a timely reply to the Office Action mailed December 4, 2003. In fact, applicant filed a timely reply by facsimile transmission on June 1, 2004 and respective copies of the reply, petition for extension of time, and return receipt received by facsimile transmission on June 1, 2004 are submitted herewith. It is therefore requested that the Notice of Abandonment should be withdrawn and that this application should be restored to pending status.

Respectfully submitted,

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PAGE 1/29 * RCVD AT 6/1/2004 6:22:34 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-1/0 * DNIS:8729306 * CSID:503 574 3197 * DURATION (mm-ss):08-34

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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of

Yu-Chin HSU et al

Art Unit: 2123

Application No: 09/630,348

Examiner: Kandasamy Thangavelu

Filed: July 31, 2000

For: CIRCUIT PROPERTY VERIFICATION SYSTEM

PETITION FOR EXTENSION OF TIME UNDER 37 CFR 1.136(a)

COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450

Sir:

Applicant hereby petitions for three months' extension of time, i.e. until June 4, 2004, for reply to the Office Action dated December 4, 2003, under 37 CFR 1.136(a). Please charge the fee of $475 under 37 CFR 1.17(a)(3)(small entity) to Deposit Account 19-2560.

Respectfully submitted,

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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of

Yu-Chin HSU et al

Art Unit: 2123

Application No: 09/630,348

Examiner:
Kandasamy Thangavelu

Filed: July 31, 2000

For: CIRCUIT PROPERTY VERIFICATION SYSTEM

REPLY TO THE OFFICE ACTION MAILED 12/04/2003

COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450

Sir:

Further examination and consideration of this application are requested in view of the following Amendments and Remarks.

DESCRIPTION AMENDMENTS

Rewrite the paragraph beginning on page 1, line 37, to read as follows:

Design engineers often like to verify that a circuit has one or more particular properties. We say a circuit possesses a "property" if it always exhibits a particular consequent behavior following a particular antecedent event. An "antecedent event" can be any particular pattern in any combination of the circuit's input, output and internal signals. A "consequent ~~event~~ behavior" can be any particular pattern in any combination of the circuit's output and internal signals. Note that a consequent behavior involves only the signals that the circuit generates (output and internal) and does not involve the input signals that the circuit receives. Thus once an antecedent event occurs, the circuit having a particular property will exhibit the consequent behavior regardless of the behavior of its input signals following the antecedent event. To fully verify that a circuit has a particular property, we must verify that the circuit will exhibit a particular consequent behavior in response to an antecedent event regardless of the behavior of any of its input signals following the antecedent event.

Rewrite the paragraph beginning on page 4, line 29, to read as follows:

The system also generates a temporally expanded model of the circuit whenever the antecedent detector detects an occurrence of the antecedent event. The temporally expanded circuit model represents the circuit as a set of N circuit functions CKT_1-CKT_N, each corresponding to a separate one of the N clock cycles following the antecedent event in which the consequent behavior occurs. The Kth circuit function CKT_K has a first input variable IN_{K-1} representing the states of the circuit's input signals at the start of clock cycle k. A second input variable $STATE_{K-1}$ of function CKT_N represents the states of internal or output signals defining the state of the circuit at the end of clock cycle K-1. Each circuit function CKT_K produces an output variable CB_K representing the state of any ~~each~~ signal that may be included in the definition of the consequent behavior during clock cycle K, and an output variable $STATE_K$ representing the state of the circuit during clock cycle K. The sampled state of the simulated

circuit forms the $STATE_0$ of the input variable to circuit function CKT_1. Thus

$$(CB_K, STATE_K) = CKT_K(IN_{K-1}, STATE_{K-1})$$

Rewrite the paragraph beginning on page 8, line 4, to read as follows:

FIG. 2 illustrates the behavior of counter 10 during an example sequence of input signal state changes as might be defined by a test bench. At starting time 0, counter 10 is in state 0. The test bench drives the COUNT signal true (C) and drives the RESET signal false (/R) before the next CLOCK signal edge so that at time 1 counter 10 moves to state 1. The RESET signal is then set true (R) ~~with~~ and the count signal is set false (/C) before the CLOCK signal edge at time 2 so that counter 10 returns to state 0 at time 2. The test bench then sets the COUNT signal true and RESET signal false (C & /R) for the next two clock cycles so that counter 10 advances to states 1 and 2 at times 3 and 4. The test bench then sets the RESET signal true and the COUNT signal false (R & /C) to reset counter to state 0 at time 5.

Rewrite the paragraph beginning on page 11, line 29, to read as follows:

FIG. 3 illustrates a BDD state space model 12 of counter 10 of FIG. 1 that might be generated by a conventional state space model generation tool. The state space model is "exhaustive" because it includes every state to which counter circuit 10 could be driven and indicates the input signal combinations that instigate every possible state transition. For example, the model of FIG. 3 indicates that the circuit can transition from state 0 to state 1 on a CLOCK signal edge only if the COUNT signal is true and the RESET signal is false (C & \R). Circuit 10 responds to the other three RESET and COUNT signal state combinations by remaining in state 0. FIG. 3 shows circuit 10 transitions from state 1 to state 0 if RESET is true and COUNT is either true or false (R & C) or (R & /C) circuit 10 transitions from state 1 to state 2 if RESET is false and COUNT is true (/R & C) and stays in state 1 if both RESET and COUNT signals are false (/R & /C). The model of ~~FIG. 2~~ FIG. 3 similarly defines all transitions from states 2-7.

Rewrite the paragraph beginning on page 14, line 12, to read as follows:

Upon recording the sampled state of counter 10 on each occurrence of the antecedent event during the simulation, the property verification system determines whether the circuit, starting in the sampled state, will exhibit the consequent behavior under all input signal conditions that might occur within the time allotted for the consequent behavior. In this example the consequent behavior (returning to state 0) must occur in the next clock cycle following the antecedent event. Thus the scope of the property verification investigation is restricted to what the counter circuit might do in the next cycle in response to all combinations of input signal states when in the sampled states 1 and 2.

Rewrite the paragraph beginning on page 16, line 37, to read as follows:

Process 30 samples the simulator's OUTPUT waveform data at the time the antecedent event occurs to determine the current state of the ~~simulate~~ simulation circuit. Process 30 then creates a "temporally expanded" model of the circuit, and analyzes the model to determine whether the circuit defined by the HDL file will exhibit the consequent behavior defined by a user-provided consequent behavior specification within the number N of clock cycles allotted for the consequent behavior beginning in its sampled state regardless of the behavior of the circuit input signals during those N cycles.

Rewrite the paragraph beginning on page 18, line 28, to read as follows:

However implementing each function CKT_1-CKT_N using the generic function illustrated in FIG. 8 would require more processing time and resources than needed in order to verify the property. Since the definition of the consequent behavior normally will not include behavior of every circuit signal H-P during every one of the N clock signal cycles, the variables CB_1 - CB_N provided to detector 34 of FIG. 7 do not need to ~~represents~~ represent the state of every one of those signals H-P. Functions CKT_1-CKT_N of FIG. 7 can therefore be substantially reduced versions of the generic functions of FIG. 8.

Rewrite the paragraph beginning on page 20, line 23, to read as follows:

FIG. 11 illustrates function CKT_1 of FIG. 7. Function CKT_1 need not implement components 41, 44 or 47-49 because their output signals H, K and N-P have no influence on the input variable $STATE_1$ for function CKT_2 (FIG. 10) or on the CB_1 input to consequent behavior pattern detector 34 (FIG. 7). Although the output state variable $STATE_1$ of function CKT_1 must represent the output of component 45, the value of that signal will always be a constant function of the sampled values of signals J and L. Thus it is not necessary for function CKT_1 to model ~~competent~~ component 45.

Rewrite the paragraph beginning on page 20, line 33, to read as follows:

FIG. 12 represents the resulting temporarily expanded circuit model that is implemented by a single function combining all of functions CKT_1-CKT_3 of FIGs. 9-11. Note that since the value L_1 of state signal L at the end of clock cycle N = 1 and the value H_0 of state signal H at the end of clock cycle N = 0 are constant functions of the sampled state of the simulated circuit. Note that the temporally expanded circuit model of FIG. 12 has only 5 input signals, the A_0-D_0 signals for clock cycle N = 1 and the G_2 signal for clock cycle N = 3. None of the other input signals for clock cycles N = 1 to 3 have any influence on the state of output signal P_3 at the end of clock cycle N = 3. The computing resources and time needed to implement and investigate the behavior of output signal P_3 at the clock cycle N = 3 in response to various combinations of input signals during cycle N = 1 to 3 are greatly reduced because the total number of bits of circuit function input variables IN_0 and IN_2 has been reduced from 21 to just 5. The system therefore need only investigate function response to ~~only 2_5 (32)~~ only 25 (32) input variable combinations instead of 2_{21} (2,097,152) possible input variable combinations.

Rewrite the paragraph beginning at page 22, line 14, to read as follows:

Thus has been shown and described a system for verifying that a circuit specification describes a circuit that ~~specification~~ will

exhibit a particular property. While the forgoing specification has described a preferred embodiment of the present invention, one skilled in the art may make many modifications to the preferred embodiment without departing from the invention in its broader aspects. The appended claims therefore are intended to cover all such modifications as fall within the true scope and spirit of the invention.

CLAIM AMENDMENTS

1. (Currently Amended) A method for verifying that a circuit described by a circuit specification as receiving and processing input signals to produce output signals has a property of responding to a first pattern in its input signals by producing a second pattern in its output signals within a finite time, the method comprising the steps of:

a. simulating operation of the circuit described by the circuit specification to produce output waveform data representing behavior of the circuit's input and output signals and representing a state of the circuit, wherein the output waveform data represents at least one occurrence of said first pattern in the input signals; and

b. determining a current state of the circuit from said output waveform data whenever the output waveform data represents an occurrence of the first pattern in the input signals, and

c. processing said circuit specification to determine whether, starting from each current state determined in step b, the circuit it describes will exhibit said second pattern within that finite time under all possible combinations of input signal states during said finite time.

2. (Currently Amended) An apparatus for verifying that a circuit specification describes a circuit exhibiting a property defined as a consequent behavior occurring during clock cycles 1 - N of a clock signal following an antecedent event, wherein N is an integer greater than 0, wherein the circuit responds to input signals by producing output signals, wherein the antecedent event is a first state change pattern in at least one of the input and output signals, and wherein the consequent behavior is production of a second state change pattern in at least one of the output signals, the apparatus comprising:

a circuit simulator for implementing a simulated circuit, wherein the simulated circuit simulates the circuit described by the circuit specification, wherein the circuit simulator produces output waveform data representing time-varying behavior of the input and output signals and representing a current state of the simulated circuit;

detector means for detecting in the output waveform data an occurrence of a data pattern representing the antecedent event; and

means for generating a temporally-expanded model of the simulated circuit based on the circuit specification and on a state of the circuit upon the occurrence of the data pattern as indicated by the output waveform data, representing the circuit as a set of N circuit functions CKT_1-CKT_N, each corresponding to a separate one of the N clock cycles and each representing behavior of the circuit during its corresponding clock cycle.

3. (Original) The apparatus in accordance with claim 2 wherein the Kth circuit function CKT_K (for K = 1 to N) has a first input variable representing states of circuit input signals at a start of clock cycle K that influence the consequent behavior.

4. (Original) The apparatus in accordance with claim 3 wherein the Kth circuit function CKT_K (for K = 1 to N) has a second input variable representing states of circuit output signals at the start of clock cycle K that influence the consequent behavior.

5. (Original) The apparatus in accordance with claim 4 wherein the Kth circuit function CKT_K (for K = 1 to N-1) has a first output variable representing states of circuit output signals at an end of clock cycle K that influence the consequent behavior.

6. (Currently Amended) The apparatus in accordance with claim 5 wherein the Kth circuit function CKT_K (for K = 1 to N-1) has a second output variable representing states of any circuit output signals at the end of clock ~~cycle k~~ cycle K that are included in the second state change pattern.

7. (Original) The apparatus in accordance with claim 6 further comprising means for receiving and analyzing the second output variable of each of the circuit functions to verify whether the circuit exhibits the consequent behavior.

8. (Original) A method for verifying that a circuit specification describes a circuit exhibiting a property defined as a consequent behavior occurring during clock cycles 1-N of a clock signal following an antecedent event, wherein N is an integer greater than 0, wherein

the circuit responds to input signals by producing output signals, wherein the antecedent event is a first state change pattern in at least one of the input and output signals, and wherein the consequent behavior is production of a second state change pattern in at least one of the output signals, the method comprising the steps of:

a. simulating behavior of the circuit described by the circuit specification to produce output waveform data representing time-varying behavior of the input and output signals and representing a current state of the simulated circuit;

b. generating upon each occurrence of a data pattern in the output waveform data representing the antecedent event, a temporally-expanded model of the simulated circuit representing the circuit as a set of N circuit functions CKT_1-CKT_N, each corresponding to a separate one of the N clock cycles,

9. (Currently Amended) The ~~apparatus~~ method in accordance with claim 8 wherein the Kth circuit function CKT_K (for K = 1 to N-1) has a first output variable representing states of circuit output signals at an end of clock cycle K that influence the consequent behavior.

10. (Currently Amended) The ~~apparatus~~ method in accordance with claim 9

wherein the Kth circuit function CKT_K (for K = 1 to N-1) has a second output variable representing states of any circuit output signals at the end of clock cycle ~~k~~ K that are included in the second state change pattern.

11. (Currently Amended) The ~~apparatus~~ method in accordance with claim 10 further comprising ~~means for~~ for the step of:

c. receiving and analyzing the second output variable of each of the circuit functions to verify whether the circuit exhibits the consequent behavior.

12. (Original) The method in accordance with claim 11 wherein the Kth circuit function CKT_K (for K = 1 to N) has a first input variable representing states of circuit input signals at a start of clock cycle K that influence the consequent behavior.

13. (Currently Amended) The ~~apparatus~~ method in accordance with claim 12 wherein the Kth circuit function CKT_K (for K = 1 to N) has a second input variable representing states of circuit output signals at the start of clock cycle K that influence the consequent behavior.

14. (Original) An apparatus for verifying that a circuit specification describes a circuit exhibiting a property defined as a consequent behavior following an antecedent event, wherein the circuit responds to input signals by producing output signals, wherein the antecedent event is a first state change pattern in at least one of the input and output signals, and wherein the consequent behavior is a second state change pattern in at least one of the output signals, the apparatus comprising:

a circuit simulator for implementing a simulated circuit, wherein the simulated circuit simulates the circuit described by the circuit specification, wherein the circuit simulator produces output waveform data representing time-varying behavior of the input and output signals and representing a current state of the simulated circuit;

detector means for detecting in the output waveform data an occurrence of a data pattern representing the antecedent event;

means for generating a state space model of the simulated circuit representing states of the simulated circuit that are reachable from the current state of the simulated circuit represented by the circuit simulator output waveform data when the detector means detects the data pattern representing the antecedent event; and

means for analyzing the state space model to verify the circuit exhibits the consequent behavior.

15. (Currently Amended) The apparatus in accordance with claim 14

wherein the circuit transitions between states only on edges of a periodic clock signal supplied as input thereto, and

wherein the consequent behavior occurs during a finite number of periods of the clock signal following the antecedent event~~, and~~

~~wherein the state space model represents all states of the simulated circuit that are reachable from the current state of the simulated circuit represented by the circuit simulator output data within the finite number of clock signal cycles after the detector means detects the data pattern representing the antecedent event~~.

16. (Currently Amended) The apparatus in accordance with claim 15 wherein the state space model represents ~~all~~ only states of the simulated circuit that are reachable from the current state of the simulated circuit represented by the circuit simulator output data within the finite number of clock signal cycles after the detector means detects the data pattern representing the antecedent event.

17. (Original) A method for verifying that a circuit specification describes a circuit exhibiting a property defined as a consequent behavior following an antecedent event, wherein the circuit responds to input signals by producing output signals, wherein the antecedent event is a first state change pattern in at least one of the input and output signals, and wherein the consequent behavior is a second state change pattern in at least one of the output signals, the method comprising the steps of:

simulating the circuit to produce waveform data representing successive state changes of the input and output signals and representing successive states of the circuit;

generating a state space model of the circuit including states of the circuit that are reachable from a state of the circuit represented by the waveform data when the data represents the antecedent event; and

analyzing the state space model to verify the circuit exhibits the consequent behavior.

18. (Original) The method in accordance with claim 17

wherein the circuit transitions between states only on edges of a periodic clock signal supplied as input thereto,

wherein the consequent behavior occurs during a finite number of periods of the clock signal following the antecedent event, and

wherein the generated state space model includes all states of the circuit that are reachable from the current state of the circuit represented by the waveform data within the finite number of periods of the clock signal after the waveform data represents the antecedent event.

19. (Original) The method in accordance with claim 17 wherein the generated state space model includes only states of the circuit that

are reachable from the current state of the circuit represented by the waveform data within the finite number of periods of the clock signal after the waveform data represents the antecedent event.

REMARKS

The following numbered sections are provided in response to similarly numbered sections of the office action.

1, 2, 3. No response is required.

4. The specification is amended in response to the Examiner's objections. No new matter is added.

5,6. Claims 6, 7 and 10-13 are amended in response to the Examiner objections.

7,8 Claims 9-13 are rejected under 35 U.S.C. 112, second paragraph and in response claims 9-13 are amended. Claim 16 is objected to under 37 CFR 1.75 as being a substantial duplicate of claim 15, and in response claim 15 is amended.

9. No response is required.

10, 11, 12. Claims 1 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent 5,905,833 (KA) in view of U.S. patent 5,513,122 (CH). The Examiner is respectfully requested to withdraw the rejection of claims 1 and 14 in view of the following comments distinguishing those claims over the combination of KA and CH

Claim 1

The invention as recited in claim 1 relates to a method for verifying a property of a circuit described by a circuit specification. The conventional approach to verifying circuit properties is to use a simulator to generate waveform data representing behavior of its input, output and internal signals and to study that waveform data to determine whether the circuit exhibits various properties. This is the approach taught by KA. A circuit simulator 102 (FIG. 1) simulates operation of a circuit described by a specification 106 in response to an input signal pattern 140 specified by a test bench 104. The test bench 104 also includes a verification engine 136 that looks for various signal patterns in the waveform data output of simulator 102 to verify whether the simulated circuit

behaves as expected. Simulation works well for verifying certain types of circuit properties and behaviors but not for others.

The invention is concerned with verifying a particular property of a circuit. Suppose a designer wants to verify that a circuit described by a specification has the following property:

> If the simulated circuit is driven to some particular state and then stimulated with a particular input signal pattern (the recited "first pattern"), then the simulated circuit will produce a particular output signal pattern (the recited "second pattern") within some time interval T thereafter, regardless of how the input signals might behave during interval T.

In order to verify this property using a simulator, it would be necessary to repeatedly do the following:

1. drive the simulated circuit to the particular state,
2. apply the first pattern of input signals to the circuit,
3. apply some pattern of input signals during interval T, and
4. check to see if the output signals exhibit the expected second pattern during time interval T.

How many times would a simulator have to repeat this four-step procedure (using a different pattern for each pass through step 3) to ensure that no pattern of input signals applied during step 3 would affect the ability of the circuit to produce the second pattern in its output signals during interval T? Possibly millions or billions of times, depending on how many different kinds of patterns the input signals could exhibit during that time interval. For example, if the circuit has 16 input binary input signals, and interval T is 8 clock cycles during which each input signal could be of either state, then the input signals could exhibit 2^{128} different patterns during that interval. Thus in most situations it is impractical to use a simulator alone to verify this kind of property. It would take too much time for the simulator to perform the simulation, and too much time to check the simulator output data to determine whether the circuit exhibits the desired property.

In the applicant's verification system, as recited in claim 1, a simulator is used (step a) to simulate the circuit's behavior at least up to the point where it reaches the state of interest and is stimulated with the first pattern. At that point, the waveform data output of the simulator is checked (step b), but only to determine the state of the circuit at that point. The applicant is not using the simulator output data to determine whether the circuit has the property of interest.

Once the state of the circuit is known, the applicant's method then (step c) . processes the circuit specification to determine whether, starting from [that state] the circuit will exhibit the second pattern within a finite time under all possible combinations of input signal states during the finite time. Thus, rather than looking at the simulator output, the applicant's method of claim 1 processes the specification in some way to determine whether starting at the indicated state, the circuit will always produced the second pattern in its output signals regardless of what the input signals might do.

Thus, the applicant does not check the simulator waveform data output to see how the circuit behaves after it is stimulated with the first pattern of input signals to determine whether it exhibits the desired property. The applicant's method (step c) processes the specification in some (more efficient) way to determine that, but to do so it is necessary to know the state of the circuit at the time it is to be stimulated with the first pattern of input signals. That is what the simulator is used for in step a, merely to drive the simulated circuit to some state and provide output data representing that state (step b).

The Examiner correctly points out that KA teaches step a.

The Examiner correctly points out that KA does not teach step b.

The Examiner's position with respect to whether KA teaches step c is ambiguous. The first sentence of the first full paragraph of page 10 of the office action states that KA teaches step c while the next sentence of the office action states KA does not teach step b. For purposes of this response, the applicant assumes the Examiner is of the opinion that KA teaches step c. Claim 1, step c reads as follows:

"c. processing said circuit specification to determine whether, starting from each current state determined in step b, the circuit it describes will exhibit said second pattern within that finite time under all possible combinations of input signal states during said finite time."

It is clear from the wording of step c that performance of step c is not possible without prior performance of step b. Since the Examiner correctly points out that KA does not describe a method that carries out step b, it is not possible for KA to describe a method that carries out step b.

The Examiner incorrectly cites CH (Abstract, L6-11, and L14-15) as teaching the subject matter of step b,

"b. determining a current state of the circuit from said output waveform data whenever the output waveform data represents an occurrence of the first pattern in the input signals".

The cited lines of CH talk about an operator or a data file as providing an "initial configuration" (i.e., initial states) of a digital system (such as a circuit), but do not teach determining a current state of a circuit from the waveform data output of a simulator simulating that circuit as recited in claim 1. What states should the operator choose as the initial states and how can the operator obtain the data characterizing those states? Those are not trivial questions since the choice of initial states upon which to base the analysis provided by CH is a very important determinant as to whether the state space analysis method taught by CH will provide useful information about a circuit. If an initial state is not a state that the circuit is ever likely to enter, then determining the states it might reach from that unlikely state is a useless exercise. **CH doesn't suggest how the operator ought to obtain the initial configuration state data or how to produce the "data file" containing that state data.**

The applicant teaches, and claim 1 recites, to obtain the initial state data from the output data of a circuit simulator. The simulator typically stimulates a circuit model with input signal patterns the

circuit is likely to encounter in normal use and therefore drives the circuit to the normal states the circuit likely to enter during normal operation. Step c investigates whether the circuit, starting in of the normal states it entered during the simulation, might fail to respond appropriately to a particular input pattern it received at that point, if it subsequently receives an unexpected input signal pattern - some pattern not presented during the simulation. Thus combining the two types of circuit analysis systems in this manner renders them complementary in that together they provide a more comprehensive view of circuit behavior. The analysis provided at step c fills in some gaps in knowledge about circuit behavior that cannot be obtained from the simulation results.

The Examiner indicates it would have been obvious to extract the initial state data supplied as input to CH's method from the waveform data output of a simulator because "that would provide the initial configurations of the states and variables values." However, but the fact that circuit state data can be obtained from a simulator output is not sufficient grounds for declaring it obvious for one of skill in the art to that one should use simulator output as a source of input state data for CH's circuit analysis method. The mere fact that any or all of the parts of an invention exist in the prior art does not render the invention, as a combination of such old parts, obvious. Circuit simulation and state space analysis are two completely different methods for assessing circuit behavior, and neither KA nor CH provides any indication that the two analysis methods could or should be combined in some beneficial way. To justify combining KA and CH, the Examiner must show that the cited references motivate one of skill in the art to combine those two different analysis techniques - in particular to run a circuit simulation, to process the output of the circuit simulation to determine a set of initial states of the circuit in which it was stimulated by a particular input signal pattern, and to carry out CH's state space analysis method based on initial states determined from the simulator output. The Examiner has not made such a showing. It is not enough to simply point out that state data can be derived from a simulator's output data. There must be a showing that the prior art teaches or suggests that is how it should be obtained.

The Examiner incorrectly asserts CH teaches step c:

> "c. processing said circuit specification to determine whether, starting from each current state determined in step b, the circuit it describes will exhibit said second pattern within that finite time under all possible combinations of input signal states during said finite time."

CH teaches a method and apparatus for determining the states of a circuit that are reachable from a predetermined initial state. Given an initial circuit state, the method finds the states to which the circuit can be driven given any arbitrary input signal pattern over any infinitely long period of time. See column 2, line 67 through column 3, line 4. That is not what the applicant's claim 1, step c does. Step c doesn't determine what states are reachable at <u>any</u> time from an initial state; step c determines whether a circuit will always generate a particular output signal pattern <u>within a finite time interval</u> after being stimulated with a particular input signal pattern while in a particular input state. The Examiner points out CH teaches that the state space model thus obtained can be analyzed to determine various properties of the circuit. But CH does not teach or suggest that the property tested by step c is one of them. Thus the scope of analysis CH teaches and the scope of analysis claim 1, step c recites differ with respect to the temporal limitation on states reached and also on the nature of what is being determined.

Thus while KA teaches step a of claim 1, neither KA nor CH teaches or suggests steps b or c of claim 1 and, in any case, nothing in KA or CH would motive one of skill in the art to combine their teachings regarding two such different types of circuit analysis. Claim 1 is therefore patentable over the combination of KA and CH.

Claim 14

The Examiner correctly cites KA (FIG. 1, item 102) as teaching the circuit simulator element of claim 14.

The Examiner correctly observes that while KA teaches <u>a</u> detector means, KA fails to teach the recited detector means for detecting a data pattern in a simulator's waveform data output representing an antecedent event that is a "<u>state change pattern</u>" in at least one

circuit input or output signal. However, the Examiner incorrectly cites CH (Abstract, L6-11 and L14-15) as teaching this. The Abstract of CH teaches only that an operator or a data file specify a set of initial states of a digital system and that it is possible to make a model of the digital system to determine the states the digital system can reach from those initial states. Nothing in CH teaches anything about checking the output waveform data of a simulator for a particular state change pattern in a circuit input or output signal.

The applicant's invention of claim 14 that includes a circuit simulator as taught by KA and a state space generator and analyzer as taught by CH. However the Examiner presents insufficient grounds for asserting that it would be obvious to one of skill in the art to combine a circuit simulator with a state space generator and analyzer as recited in claim 14. The Examiner seeks to justify the obviousness of the invention of claim 14 with the following statement:

> "It would have been obvious to one of ordinary skill in the art ... to modify the apparatus of KA with the apparatus of CH ... as that would allow the user to determine if a given specification produced unexpected results; and allow verifying that the design of the circuit met specified operation correctness and performance criteria within specified time frames."

Thus, the Examiner maintains that it would be obvious to combine the parts taught by KA and CH to produce the claimed invention simply because doing so would result in a useful apparatus. But the mere fact that a combination of old parts would be useful does not render the combination obvious. The utility of an invention is a requirement for its patentability, not a justification for declaring it unpatentable.

A simulator and a state space analyzer are two different circuit analysis tools that operate in very different manners to determine different types of information about a circuit. To justify a rejection on the basis of the obviousness of combining those two tools in the manner recited in claim 14, the Examiner must cite references that motivate one of skill in the art to combine a circuit simulator as taught by KA with a state space generator and analyzer as taught by CH to arrive at a new circuit analysis apparatus as recited in claim 14.

Simply stating that one of skill in the art would find such a combined circuit analysis apparatus to be useful does not meet that burden. Claim 14 is therefore patentable over the combination of KA and CH.

13. Claims 2-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over KA in vie of CH and U.S. patent 6,138,266 (GA). The Examiner is respectfully requested to withdraw the rejections of these claims in view of the following comments distinguishing them over the cited references.

Claim 2

Claim 2 recites an apparatus for verifying that a circuit specification describes a circuit that produces a "second state change pattern" in at least one of the output signals.
during N clock cycles following an antecedent event that is a "first state change pattern" in at least one of the circuit's input and output signals.

The Examiner correctly observes that while KA teaches a detector means, KA fails to teach the recited detector means for detecting a data pattern in a simulator's waveform data output representing an antecedent event that is a "state change pattern" in at least one circuit input or output signal. However, the Examiner incorrectly cites CH (Abstract, L6-11 and L14-15) as teaching the detector means. The Abstract of CH teaches only that an operator or a data file specify a set of initial states of a digital system and that it is possible to make a model of the digital system to determine the states the digital system can reach from those initial states. Nothing in CH teaches anything about checking the output waveform data of a simulator for a particular state change pattern in a circuit input or output signal.

The Examiner correctly states that KA does not teach the recited "means for generating a temporally expanded model of the simulated circuit representing the circuit as a set of N circuit functions CKT_1-CKT_N, each corresponding to a separate one of the N clock cycles and each representing behavior of the circuit during the corresponding clock cycle."

A "temporally expanded model" of a circuit, as illustrated in the applicant's FIG. 7, is a rather unusual circuit model that includes N

models of the same circuit, each modeling circuit behavior during a different one of N successive clock cycles so that successive states of the circuit appear in the model to occur concurrently. In other words, a temporality expanded model of a circuit does in one clock cycle what a conventional circuit model does in N clock cycles, because it includes N versions of the circuit, each doing what the circuit does during a separate clock cycle, but all working concurrently. See the applicant's specification page 17 for a detailed description of the nature of a "temporarily expanded circuit model".

The Examiner points to FIG. 2 of GA as showing such a temporally expanded model of a circuit. But FIG. 2 depicts only a conventional circuit model in which some of the combinational logic appears in block form. The Examiner also points to GA column 2, lines 25-50 as teaching a temporally expanded circuit model. But this section of GA talks only about breaking a circuit design into several separate blocks of combinational logic interconnected through flip-flops and has nothing to do with temporally expanded circuit model of the type recited in claim 2. The Examiner points to FIG. 17A of GA and column 24, lines 15-64 as showing or discussing a temporally expanded model of a circuit, but FIG. 17A and that section of GA show or discuss only a conventional block diagram of a circuit where each block represents a different <u>part</u> of the circuit. The blocks do not represent behavior of the <u>same</u> circuit at different <u>times</u>, as is the case for a temporally expanded circuit model.

Claim 2 is therefore patentable over the combination of KA, CH and GA because none of the reference teaches the recited detector means and none of the recited references teaches the recited means for generating a temporally expanded model of the simulated circuit."

Claim 3

Claim 3 depends on claim 2 and is patentable over the cited references for similar reasons. Claim 3 further recites, " the Kth circuit function CKT_K (for K = 1 to N) has a first input variable representing states of circuit input signals at a start of clock cycle K that influence the consequent behavior". For example the applicant's FIG. 7 shows N blocks CKT_1-CKT_N each representing behavior of the <u>same</u> circuit but during a different clock cycle. As recited

in claim 3, the input (IN_k) of each K^{th} circuit CKT_k represents states of circuit input signals during clock cycle K. The Examiner incorrectly points to GA (FIG. 2) as teaching this. FIG. 2 is a conventional schematic diagram with blocks 210, 220 and 230 representing separate parts of a circuit. They do not all represent behavior of the same circuit during different clock cycles as recited in claim 2, and blocks 210,220,230 receive input variables 201-203 representing states of separate input signals during the same clock cycle - they do not receive input variable representing states of the same signals during different clock cycles as recited in claim 3.

Claim 4

Claim 4 depends on claim 3 and is patentable over the cited references for similar reasons. Claim 4 further recites, "wherein the Kth circuit function CKT_K (for K = 1 to N) has a second input variable representing states of circuit output signals at the start of clock cycle K that influence the consequent behavior". For example see the applicant's FIG 7 wherein each circuit function CKT_K has an input variable $STATE_{K-1}$ representing states of the circuit's output signals at the start of clock cycle K. The Examiner again cites GA, FIG. 2, as teaching this. But, as discussed above, FIG. 2 is a conventional circuit model, not a temporally expanded circuit model. The inputs of blocks 210, 220, 230 represent states of separate input signals; they do not represent states of the same set of circuit output signals at the start of separate clock cycles as recited in claim 4.

Claim 5

Claim 5 depends on claim 4 and is patentable over the cited references for similar reasons. Claim 5 further recites, "the Kth circuit function CKT_K (for K = 1 to N-1) has a first output variable representing states of circuit output signals at an end of clock cycle K that influence the consequent behavior." For example see the applicant's FIG 7 wherein each circuit function CKT_K has an output variable $STATE_K$ representing states of the circuit's output signals at the end of clock cycle K. The Examiner again cites GA, FIG. 2, as teaching this. But, as discussed above, FIG. 2 is a conventional circuit model, not a temporally expanded circuit model. The outputs of blocks 210, 220, 230 represent states of separate signals; they do

not represent states of the same set of circuit output signals at the end of separate clock cycles as recited in claim 5.

Claim 6

Claim 6 depends on claim 5 and is patentable over the cited references for similar reasons. Claim 6 further recites, "the Kth circuit function CKT_K (for K = 1 to N-1) has a second output variable representing states of any circuit output signals at the end of clock cycle K that are included in the second state change pattern." For example see the applicant's FIG 7 wherein each circuit function CKT_K has an output variable CB_K representing states of circuit output signals at the end of clock cycle K that are included in the second state change pattern. The Examiner again cites GA, FIG. 2, as teaching this. But, as discussed above, FIG. 2 is a conventional circuit model, not a temporally expanded circuit model. The outputs of blocks 210, 220, 230 represent states of separate signals; they do not represent states of the same set of circuit output signals at the end of separate clock cycles as recited in claim 6. The Examiner correctly notes that in GA, FIG. 2, signals pass from one block to another on a cycle-by-cycle basis,.but that is precisely not what happens in the temporally expanded circuit model of claims 2-6. Note that circuit functions CKT_K are not clocked.

Claim 7

Claim 7 depends on claim 6 and is patentable over the cited references for similar reasons. Claim 7 further recites, "means for receiving and analyzing the second output variable of each of the circuit functions to verify whether the circuit exhibits the consequent behavior." This reads on block 34 of FIG. 7. Note that the model of FIG. 7 requires only one clock cycle to generate data CB_1 - CB_N representing the output signal pattern produced by the circuit being modeled over a period of N clock cycles. Thus pattern detector 34 can detect an N-cycle consequent behavior pattern in only one clock cycle. The temporally expanded model of FIG. 7 therefore speeds up the verification process. The Examiner cites GA, column 7, lines 57-62 as teaching the recited means for receiving and analyzing, but this section of GA has nothing to do with detecting behavior patterns in a circuit's output signals.

Claims 8-13

Claims 8-13 are patentable over the combination of KA, CH and GA for reasons similar to those discussed above in connection with claims 2, 5-7, 3 and 4.

14. Claims 15 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over KA in view of CH and further in view of U.S. patent 6,009,653 (SE). The Examiner is respectfully requested to withdraw the rejections of claims 15 and 16 in view of the following comments distinguishing these claims over the cited references.

Claim 15

Claim 15 depends on claim 14 and is patentable over the combination of KA and CH for similar reasons. Claim 15 further recites, "the circuit transitions between states only on edges of a periodic clock signal supplied as input thereto, and ... the consequent behavior occurs during a finite number of periods of the clock signal following the antecedent event." The Examiner correctly cites SE as disclosing a circuit that transitions between state only on edge of a periodic signal. However nothing in SE overcomes the lack of teaching in KA and CH of the subject matter of parent claim 14.

Claim 16

Claim 16 depends on claim 15 and is patentable over the combination of KA, CH and SE for similar reasons. Claim 16 (as amended) further recites, "the state space model represents only states of the simulated circuit that are reachable from the current state of the simulated circuit represented by the circuit simulator output data within the finite number of clock signal cycles after the detector means detects the data pattern representing the antecedent event." The Examiner indicates CH teaches the additional subject matter of claim 16, but CH teaches generating a state space model representing all reachable states, not just the states that are reachable within a finite number of clock cycles after some detected antecedent event, as recited in claim 16.

15. Claims 17 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over KA in view of CH and in further view of U.S. patent

6,449,752 (BA). The examiner is respectfully requested to withdraw the rejection of claims 17 and 19 in view of the following comments distinguishing these claims over the cited references.

Claim 17

Claim 17 recites a method for verifying that a circuit specification describes a circuit exhibiting a property defined as a consequent behavior following an antecedent event, including steps of:

> "simulating the circuit to produce waveform data representing successive state changes of the input and output signals and representing successive states of the circuit;
>
> generating a state space model of the circuit including states of the circuit that are reachable from a state of the circuit represented by the waveform data when the data represents the antecedent event; and
>
> analyzing the state space model to verify the circuit exhibits the consequent behavior."

KA and BA disclose or suggest the step of "simulating the circuit to produce waveform data."

The Examiner correctly cites CH as disclosing a method for generating a state space model including states of a circuit that are reachable from an initial state. But none of the cited references teaches that the initial states supplied as inputs to CH's state space modeling method should be derived from the waveform data output of a simulator as recited in claim 17. . The Examiner seeks to justify the obviousness of the invention of claim 17 with the following statement:

> "It would have been obvious to one of ordinary skill in the art … to combine the method of KA with the method of CH … as that would allow the user to determine if a given specification produced unexpected results; and allow verifying that the design of the circuit met specified operation correctness and performance criteria within specified time frames."

Thus, the Examiner maintains that it would be obvious to combine

the parts taught by KA and CH to produce the claimed invention simply because doing so would result in a useful method. But the mere fact that a new combination of old processes would be useful does not render the combination unpatentably obvious. The utility of an invention is a requirement for its patentability, not a justification for declaring it unpatentable.

Simulator and a state space analysis are two different circuit analysis methods that operate in very different manners to determine different types of information about a circuit. To justify a rejection on the basis of the obviousness of combining those two methods in the manner recited in claim 17, the Examiner must cite references that motivate one of skill in the art to combine a circuit simulation as taught by KA (or BA) with a state space analysis as taught by CH to arrive at a new circuit analysis method as recited in claim 17. Simply stating that one of skill in the art would find such a new method to be useful does not meet the Examiner's burden.

Claim 19

Claim 19 depends on claim 17 and is patentable over the combination of KA, CH and BA for similar reasons. Claim 19 further recites, "the generated state space model includes only states of the circuit that are reachable from the current state of the circuit represented by waveform data within the finite number of clock signal cycles after the detector means detects the data pattern representing the antecedent event." The Examiner indicates CH teaches the additional subject matter of claim 19, but CH teaches generating a state space model representing all reachable states, not only the states that are reachable within a finite number of clock cycles after some detected antecedent event, as recited in claim 19.

16. Claims 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over KA in view of CH, BA and SE. The Examiner is respectfully requested to withdraw the rejection of claim 18 in view of the following comments distinguishing these claims over the cited references.

Claim 18

Claim 18 depends on claim 17 and is patentable over the

combination of KA, CH and BA for similar reasons. The Examiner correctly cites SE as teaching a circuit that transitions between states only on edges of a periodic clock signal supplied as input thereto.

The Examiner incorrectly cites CH as teaching "the generated state space model includes all states of the circuit that are reachable from the current state of the circuit represented by the waveform data within the finite number of periods of the clock signal after the waveform data represents the antecedent event" as recited in claim 18. CH teaches generating a state space model representing all reachable states, not only the states that are reachable within a finite number of clock cycles after some detected antecedent event, as recited in claim 18.

17. No response is necessary.

It is believed that in view of the forgoing amendments and remarks that the application is in condition for allowance. Notice of Allowance is therefore respectfully requested.

Respectfully submitted,

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of

Yu-Chin HSU et al

Art Unit: 2123

Application No: 09/630,348

Examiner:
Kandasamy Thangavelu

Filed: July 31, 2000

For: CIRCUIT PROPERTY VERIFICATION SYSTEM

HOLDING

PETITION TO WITHDRAW ~~HOLD~~ OF ABANDONMENT

COMMISSIONER FOR PATENTS
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The records of the PTO Office should be updated

Sir:

The Notice of Abandonment mailed December 23, 2004 indicates that applicant failed to file a timely reply to the Office Action mailed December 4, 2003. ~~has been received~~ In fact, applicant filed a timely reply by facsimile transmission on June 1, 2004 and respective copies of the reply, petition for extension of time, and return receipt received by facsimile transmission on June 1, 2004 are submitted herewith. It is therefore requested that the Notice of Abandonment should be withdrawn and that this application should be restored to pending status.

Respectfully submitted,

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